BMC Mainframe: z/OS System Anatomy Part 1 - z Architecture

COURSE ABSTRACT

COURSE CODE

» MGRS-ZSA1-2021

APPLICABLE VERSIONS

» Not Applicable

DELIVERY METHOD

» Instructor-led Training (ILT)

COURSE DURATION

» 4 Days

PREREQUISITES

» A good working understanding of the z/OS environment, from a technician's perspective

RECOMMENDED TRAININGS

» NA

Course Overview

The course is developed and delivered by © RSM Technology.

This course and the follow-on Part 2 course together form the essential core of RSM's z/OS education curriculum for z/OS Systems Programmers. By attending both components attendees will gain an in-depth insight into the fundamental structure of z/OS, enabling further skills enhancement in areas such as debugging, performance, installation and customisation of the operating system.

This course concentrates on laying the ground rules of z/OS in terms of architecture and storage management, as well as explaining the major control blocks and how to interpret them. The course also introduces the major components found in today's Z Systems environments.

Target Audience

This course is designed for those who wish to gain an in-depth understanding of z/OS systems in order to improve their proficiency in the z/OS environment.

Learner Objectives

» Describe the architectural principles governing CPU, Storage and I/O
» Identify the state of a CPU and describe potential problem scenarios
» Use IPCS and the debugging guides
» Describe the principles of Virtual Storage
» Describe the purpose of AMODE and RMODE
» Describe a page fault and its consequences
» Set up a flexible paging/swapping subsystem
» Explain how dataspaces and hiperspaces work
» Describe how an IPL works
» Isolate problems during an IPL
» Explain the concept of authorised programs

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COURSE ACTIVITIES

» Classroom Presentations
» Demonstration

BMC MAINFRAME INFRASTRUCTURE AND PLATFORMS LEARNING PATH

» https://www.bmc.com/education/courses/find-courses.html#filter/%7B%22type%22%3A%22edu-specific-types-159150236%22%7D

CERTIFICATION PATHS

» This course is not part of a BMC Certification Path.

DISCOUNT OPTIONS

» Have multiple students? Contact us to discuss hosting a private class for your organization
» **Contact us for additional information**

Course Modules

Architecture

» The architectural principles of the CPU
» PSW, registers
» Interrupts system states
» PSW swapping
» Multi-processing
» Central storage
» Addressing modes
» Storage keys
» Parallel & serial channels
» Pathing
» HCD
» LCUs
» CCWs
» I/O operation
» SCSW

MVS Introduction

» The functions of the MVS operating systems
» Components required to prepare MVS for work
» Creating address spaces
» Job Entry Subsystem
» Initiators
» resource control
» Interrupt handlers and status saving
» Dispatching work
» I/O requests
» Workload Manager
» Execute the work
» Exit the work from the system

Control Blocks, Dumps & IPCS

» Using IPCS and the debugging handbooks to locate and interpret major MVS control blocks in a dump
» Finding main control blocks such as PSA, CVT, ASCB, TCB, UCB
» Main IPCS menus
» IPCS FIND command
» IPCS subcommands
» IPCS labs

Virtual Storage Concepts

» Loading programs
» Real storage problems
» DAT
» Segments & pages
» Page stealing & UIC
» Page faults
» Demand paging
» Dispatching address spaces
» Swapping & paging

MVS Storage Management

» AMODE & RMODE
» Common storage
» private storage
» Virtual Storage Manager
» Subpools
» Storage keys
» RSM
» Page faults
» Segment faults
» ASM
» Page data sets
» VIO

Dataspaces and Hiperspaces

» Primary & secondary ASC modes
» Access registers
» Using dataspaces
» VLF
» Hiperspaces

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System Initialisation

- Sysgen and IPL processes
- The function of the LOAD parameter and the LOADxx member of PARMLIB
- Concepts of authorised programs
- The subsystem interface